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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/509,086	FURBER, STEPHEN B.	
	Examiner	Art Unit	
	Adrian L. Kennedy	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2007*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31,35 and 36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31,35 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Examiner's Detailed Office Action

1. This Office Action is responsive to **Amendment After Non-Final**, filed **September 24, 2007**.

2. **This action is herby made Non-Final.**

3. **Claims 1-31 and 35-36** will be examined.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 31 is rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The claimed "tangible storage medium is critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). Appropriate correction is required.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claim 30 fails to provide a tangible result, and there must be a practical application, by either

a) **transforming (physical thing)** or

b) by having the FINAL RESULT (not the steps) achieve or produce

a using (specific, substantial, AND credible),

concrete (substantially repeatable/non-unpredictable), AND

tangible (real world/non-abstract) result.

A claim that is so broad that it reads on both statutory and non-statutory subject matter, must be amended. A claim that recites a computer that solely calculates a mathematical formula is not statutory.

The courts have also held that a claim may not preempt ideas, laws of nature or natural phenomena. The concern over preemption was expressed as early as 1852. See Le Roy v. Tatham, 55 U.S. (14 How.) 156, 175 (1852) ("A principle, in the abstract, is a fundamental truth; an original cause; a motive; these cannot be patented, as no one can claim in either of them an exclusive right."); Funk Bros. Seed Co. v. Kalo Inoculant Co., 333 U.S. 127, 132, 76 USPQ 280, 282 (1948).

Accordingly, one may not patent every "substantial practical application" of an idea, law of nature or natural phenomena because such a patent "in practical effect would be a patent on the [idea, law of nature or natural phenomena] itself." "Here the "process" claim is so abstract and sweeping as to cover both known and unknown uses of the BCD to pure-binary conversion. The end use may (1) vary from the operation of a train to verification of driver's licenses to researching the law books for precedents and (2) be performed through any existing machinery or future-devised machinery or without any apparatus." Gottschalk v. Benson, 409 U.S. 63, 71-72, 175 USPQ 673, 673 (1972).

The Courts have found that subject matter that is not a practical application or use of an

idea, a law of nature or a natural phenomenon is not patentable. As the Supreme Court has made clear, "[a]n idea of itself is not patentable." *Rubber-Tip Pencil Co. v. Howard*, 20 U.S. (1 Wall.) 498, 507 (1874); taking several abstract ideas and manipulating them together adds nothing to the basic equation. In re Warmerdam, 31 USPQ2d 1754 (Fed. Cir. 1994).

Specifically,

> The applicant's claimed invention is directed to a ***machine*** (Claims 1, 15, 16, 35), and a ***process*** (Claims 21 and 36), within the meaning of 101. (Examiner's Note: The examiner asserts that claim 16 is directed to a machine even though the applicant's claim specifically recites "a method for operating a memory" due to the fact that while the applicant's claim preamble recites a method, the applicant's claim preamble additionally states "the memory comprising" and the claim body further reciting machine components.)
>
> The applicant's claimed invention encompasses the ***abstract idea*** of a memory configuration.

Embodiment 1 (Claim 1): A memory configuration for use in a computer system.

Embodiment 2 (Claim 15): A neural network memory configuration for use in a computer system.

Embodiment 3 (Claim 16): A memory configuration for use in a computer system.

Embodiment 4 (Claim 21): A method for optimizing a computer memory in computer system.

Embodiment 5 (Claim 35): A memory configuration for use in a computer system.

Embodiment 6 (Claim 36): A method for operating a memory for use in a computer system.

The examiner takes the position that the "allocating of an identifier having a predetermined number of bits" (Embodiments 1, 3, and 4), and the "activating of address decoders" (Embodiments 2, 4, 5, and 6) cause a physical transformation to take place in the claimed embodiments. However, while the independent claims are found to be statutory, the examiner asserts that claim 30 is not statutory due to the fact that it is an attempt to patent electromagnetic signals which are natural occurring phenomena.

Therefore, **claims 1-29, 31, and 35-36 are statutory and claim 30 is not statutory**.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-12, 16-20, 30-31, and 35-36 rejected under 35 U.S.C. 102(b) as being anticipated by Jaeckel (USPN 5,113,507, referred to as Jaeckel).

Regarding claims 1:

Jaeckel teaches

a plurality of address decoders (Jaeckel: Column(C) 4, Lines(L) 18-27) each of which is allocated an identifier having a predetermined number of bits (Jaeckel: C 10, L 5-16; Examiner's Note(EN): Having not further defined the applicant's claimed "identifier" in

the claimed invention, the examiner has found that the claimed "identifier" reads on the coordinates taught by Jaeckel.), each bit having first and second selectable states; and

a data memory having a plurality of word lines of predetermined length (Jaeckel: C 20, L 10-11),

each of the said address decoders being activatable to select one of the plurality of word lines (Jaeckel: C 19, L 19-28);

the address decoders including means to receive an input address having a predetermined number of bits (Jaeckel: C 19, L 19-28; EN: Having not further defined the applicant's claimed "means to receive" in the claimed invention, the examiner has found that the claimed "means to receive" reads on the AND-Gate which makes up the address decoders as taught by Jaeckel.) and means to compare the identifier of an address decoder with the input address (Jaeckel: C 19, L 19-28; EN: Having not further defined the applicant's claimed "means to compare" in the claimed invention, the examiner has found that the claimed "means to compare" reads on the comparer which makes up the address decoders as taught by Jaeckel.); and

wherein the memory further includes means to activate an address decoder if at least a predetermined minimum number of bits set to the first selectable state in the input address correspond to bits set to the first selectable state in the decoder identifier (Jaeckel: C 19, L 19-28; EN: The examiner takes the position that the applicant's claimed "means to activate" is inherent in the invention of Jaeckel. This position is based on the fact that the address decoders are activated, which would not be possible unless there is some form of a means to activate said decoders.).

Regarding claims 2:

Jaeckel teaches

the means to compare the identifier of an address decoder with the input address considers positional correspondence between bits set to the first selectable sate in the input address and bits set to the first selectable state in the decoder identifiers (Jaeckel: C 11, L 4-7).

Regarding claims 3:

Jaeckel teaches

(Previously Presented) A memory configuration wherein each address decoder identifier has an equal number of bits set to the first selectable state (Jaeckel: C 10, L 35-38; EN: The examiner takes the position that Jaeckel anticipates the applicant's claiming of the identifiers having an equal number of bits, in teaching the matching of coordinates based on coordinates being equal.).

Regarding claims 4:

Jaeckel teaches

(Previously Presented) A memory configuration wherein the means to receive an input address is configured to receive addresses containing a predetermined number of bits set to the first selectable state (Jaeckel: C 10, L 35-38 and C 11, L 2-7; EN: The examiner takes the position that Jaeckel anticipates the applicant's claiming of a predetermined

number of bits being set to a certain state, in teaching the activation of a memory location only if the coordinates are set to the correct state.).

Regarding claims 5:

Jaeckel teaches

(Previously Presented) A memory configuration wherein the predetermined number of bits set to the first selectable state in an input address is equal to the number of bits set to the first selectable state in each of the address decoder identifiers (Jaeckel: C 11, L 55-61; EN: The examiner takes the position that Jaeckel anticipates the applicant's claiming of a predetermined number of bits being set to a certain state in the input address being equal to the bits set to a certain state in the identifier, in teaching the activation of the memory location only if input address value matches the value of the coordinates (i.e. identifier) of the memory location.).

Regarding claims 6:

Jaeckel teaches

(Previously Presented) A memory configuration wherein the data memory comprises a plurality of single bit memories, such that each bit of each word line is stored in a single bit memory (Jaeckel: C 20, L 7-10; EN: The examiner takes the position that the applicant's claimed use of single bit memory is anticipated by the use of an M-bit word for each memory address as taught by Jaeckel.).

Regarding claims 7:

Jaeckel teaches

(Previously Presented) A memory configuration wherein the data memory comprises a data input line containing an equal number of bits to each of the plurality of word lines (Jaeckel: C 19, L 19-28; EN: Having not further defined the applicant's claimed "data input line" in the claimed invention, the examiner has found that the claimed "data input line" reads on the ten inputs into the AND-Gate as taught by Jaeckel.).

Regarding claims 8:

Jaeckel teaches

(Original) A memory configuration further comprising data writing means to copy data from the data input line to word lines activated by the address decoders (Jaeckel: C 11, L 55-61; EN: Having not further defined the applicant's claimed "writing means" in the claimed invention, the examiner has found that the claimed "writing means" reads on the write operation taught by Jaeckel.).

Regarding claims 9:

Jaeckel teaches

(Previously Presented) A memory configuration wherein the data input line is configured to receive input data containing a predetermined number of bits set to the first selectable state (Jaeckel: C 10, L 35-38; EN: The examiner takes the position that Jaeckel anticipates the applicant's claiming of a predetermined number of bits being set to a

certain state, in teaching the activation of the memory location only if input address values matches the values of the coordinates.).

Regarding claims 10:

Jaeckel teaches

(Currently Amended) A memory configuration further comprising means to sum values stored at each bit of word lines activated by an address decoder to generate an activation level value for each bit (Jaeckel: C 19, L 19-28; EN: Having not further defined the applicant's claimed "means to sum" in the claimed invention, the examiner has found that the claimed "means to sum" reads on the AND-Gate taught by Jaeckel.).

Regarding claims 11:

Jaeckel teaches

means to generate an output word containing the predetermined number of bits set to the first selectable state (Jaeckel: C 20, L 7-17; EN: Having not further defined the applicant's claimed "means to generate an output word" in the claimed invention, the examiner has found that the claimed "means to generate an output word" reads on the writing (i.e. outputting) of M-bit Data words as taught by Jaeckel.).

Regarding claims 12:

Jaeckel teaches

(Original) A memory configuration wherein the bits set to first selectable state in the output are the predetermined number of bits having the highest activation level (Jaeckel: C 20, L 7-17; EN: Having not further defined the applicant's claimed "highest activation level" in the claimed invention, the examiner has found that the claimed "highest activation level" reads on the threshold values taught by Jaeckel.).

Regarding claims 16:

Jaeckel teaches

a plurality of address decoders (Jaeckel: C 4, L 18-27) each of which is allocated an identifier having a predetermined number of bits (Jaeckel: C 10, L 5-16; EN: Having not further defined the applicant's claimed "identifier" in the claimed invention, the examiner has found that the claimed "identifier" reads on the coordinates taught by Jaeckel.), each bit having first and second selectable states;

and a data memory having a plurality of word lines (Jaeckel: C 19, L 19-28) of predetermined length,

each of the said address decoders being activatable to select one of the plurality of word lines (Jaeckel: C 19, L 19-28);

wherein an input address having a predetermined number of bits is input to the address decoder, the identifier of an address decoder is compared with the input address and address decoders are activated if at least a predetermined minimum number of bits set to the first selectable state in the input address correspond to bits set to the first selectable state in the decoder identifier (Jaeckel: C 19, L 19-28; EN: The examiner takes the

position that the applicant's claimed "decoders being activated" is inherent in the invention of Jaeckel.).

Regarding claims 17:

Jaeckel teaches

(Original) A method wherein input data is presented at a data input of the data memory and the data is written to word lines activated by the activated address decoders (Jaeckel: C 11, L 55-61; EN: The examiner takes the position that Jaeckel anticipates the applicant's claimed presenting of and writing of data in teaching activation of an address decoder during read and write operations when an input address is "presented at" address decoder inputs.).

Regarding claims 18:

Jaeckel teaches

(Previously Presented) A method wherein the predetermined minimum number of bits is set such that fewer than 100 address decoders are activated by any valid input address (Jaeckel: C 10, L 35-50; EN: The examiner takes the position that in teaching that there is only one (1) way to assign values to the ten coordinates so that they all agree and teaching that an address decoder only activates when an input address's coordinates correspond to the address decoder's coordinates, Jaeckel anticipates the applicant's claiming of "fewer than 100 address decoders being activated".).

Regarding claims 19:

Jaeckel teaches

(Previously Presented) A method wherein the predetermined minimum number of bits is set such that fewer than 50 address decoders are activated by any valid input address (Jaeckel: C 10, L 35-50; EN: The examiner takes the position that in teaching that there is only one (1) way to assign values to the ten coordinates so that they all agree and teaching that an address decoder only activates when an input address's coordinates correspond to the address decoder's coordinates, Jaeckel anticipates the applicant's claiming of "fewer than 50 address decoders being activated".).

Regarding claims 20:

Jaeckel teaches

(Original) A method wherein the predetermined minimum number of bits is set such that fewer than 20 and more than 11 address decoders are activated by any valid input address (Jaeckel: C 10, L 35-50; EN: The examiner takes the position that the activating of "fewer than 20 and more than 11 address decoders", would have been obvious to one of ordinary skill in the art in light of Jaeckel teaching the activating of address decoders based on the inputting of an input address whose coordinates correspond to the coordinates of the address decoder.).

Regarding claims 30:

Jaeckel teaches

(Previously Presented) A carrier medium carrying computer readable code means to cause a computer to execute procedure in accordance with the method of claim 16 (The examiner takes the position that the means claimed by the applicant is inherent in Jaeckel teaching his invention carrying out his teachings.).

Regarding claims 31:

Jaeckel teaches

A tangible storage medium containing a computer program for carrying out the method of claim 16 (The examiner takes the position that the program claimed by the applicant is inherent in Jaeckel teaching his invention being carried out in his teachings.).

Regarding claims 35:

Jaeckel teaches,

a plurality of address decoders (Jaeckel: C 4, L 18-27) each of which is allocated an identifier having a predetermined number of bits (Jaeckel: C 10, L 5-16; EN: Having not further defined the applicant's claimed "identifier" in the claimed invention, the examiner has found that the claimed "identifier" reads on the coordinates taught by Jaeckel.), each bit having first and second selectable states;

a data memory having a plurality of word lines of predetermined length (Jaeckel: C 20, L 10-11),

each of the said address decoders being activatable to select a predetermined one of the plurality of word lines (Jaeckel: C 19, L 19-28);

the address decoders comprising means to receive an input address having a predetermined number of bits (Jaeckel: C 19, L 19-28; EN: Having not further defined the applicant's claimed "means to receive" in the claimed invention, the examiner has found that the claimed "means to receive" reads on the AND-Gate which makes up the address decoders as taught by Jaeckel.) and means to compare the identifier of an address decoder with the input address (Jaeckel: C 19, L 19-28; EN: Having not further defined the applicant's claimed "means to compare" in the claimed invention, the examiner has found that the claimed "means to compare" reads on the comparer which makes up the address decoders as taught by Jaeckel.), and

wherein the memory further comprises means to activate an address decoder if at least a predetermined minimum number of bits set to the first selectable state in the input address correspond to bits set to the first selectable state in the decoder identifier (Jaeckel: C 19, L 19-28; EN: The examiner takes the position that the applicant's claimed "means to activate" is inherent in the invention of Jaeckel. This position is based on the fact that the address decoders are activated, which would not be possible unless there is some form of a means to activate said decoders.).

Regarding claims 36:

Jaeckel teaches,

allocating to each of a plurality of address decoders (Jaeckel: C 4, L 18-27) an identifier having a predetermined number of bits (Jaeckel: C 10, L 5-16; EN: Having not further defined the applicant's claimed "identifier" in the claimed invention, the examiner has

found that the claimed "identifier" reads on the coordinates taught by Jaeckel.), each bit having first and second selectable states; and

activating each of said address decoders to select a predetermined one of a plurality of word lines in a data memory having a plurality of word lines of predetermined length (Jaeckel: C 20, L 10-11),

wherein an input address having a predetermined number of bits is input to the address decoder, the identifier of an address decoder is compared with the input address and address decoders are activated if at least a predetermined minimum number of bits set to the first selectable state in the input address correspond to bits set to the first selectable state in the decoder identifier (Jaeckel: C 19, L 19-28; EN: The examiner takes the position that the applicant's claimed "decoders being activated" is inherent in the invention of Jaeckel.).

8. Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Thewes et al. (USPN 6,037,626, referred to as Thewes).

Regarding claims 15:

Thewes teaches,

a plurality of address decoder neurons (Thewes: C 2, L 1-6; EN: The examiner takes the position that in teaching the use of a plurality of control circuits and each control circuit being equipped a respective neuron with an address decoders, the applicant's claimed

"plurality of address decoder neurons" read on the teaching of Thewes.) each of which is connected to a predetermined number of input neurons (Thewes: C 2, L 63 – C 3, L 3);

a data memory having a plurality data neurons (Thewes: C 4, L 33-42; EN: Having not further defined the applicant's claimed "data neurons" in the claimed invention, the examiner has found that the claimed "data neurons" reads on the address lines as taught by Jaeckel.); and

the address decoder neurons comprising means to receive a signal representing a firing of an input neuron to which it is connected (EN: The examiner takes the position that it is inherent for neurons to transmit signals by firing.); and

wherein an address decoder neuron comprises means to activate data neurons if firing signals are received from at least a predetermined minimum number of input neurons to which the address decoder neuron is connected (Thewes: C 4, L 33-42; EN: Having not further defined the applicant's claimed "means to activate" in the claimed invention, the examiner has found that the claimed "means to activate" reads on the enabling of a control circuit which has a neuron with an address decoder when the input address and the address of the decoder coincide as taught by Jaeckel.).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaeckel (USPN 5,113,507, referred to as Jaeckel) in view of Thewes et al. (USPN 6,037,626, referred to as Thewes).

Regarding claims 13:

Jaeckel does not teach the memory being implemented using a plurality of article neurons.

However, Thewes teaches,

(Previously Presented) A memory configuration wherein the memory is implemented using a plurality of artificial neurons connected together to form a neural network (Thewes: EN: The examiner takes the position that in teaching the use of a plurality of neurons which are interconnected in Figure 2, Thewes anticipates the applicant's claimed neural network.).

It would have been obvious to one skilled in the art at the time of invention to combine the memory system of Jaeckel with the semiconductor neuron of Thewes for the purpose of creating a neuron address decoder (Thewes: C 2, L 4-6).

Regarding claims 14:

Thewes teaches,

A memory configuration wherein the plurality of address decoders are represented by a plurality of address decoder neurons, and the data memory is represented by a plurality of

data neurons (Thewes: EN: The examiner takes the position that Thewes anticipates the applicant's claimed plurality of address decoder being represented by address decoder neurons, in his teaching of several semiconductor neuron in Column 2, Lines 30-34, and his teaching of neuron address decoders in Column 2, Lines 4-6).

11. Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaeckel (USPN 5,113,507, referred to as Jaeckel) in view of Ichiriu et al. (USPN 6,597,595, referred to as Ichiriu).

Regarding claims 21:

Jaeckel teaches

(Currently Amended) A method for optimizing the operation of a computer memory which comprises a plurality of address decoders (Jaeckel: C 4, L 18-27) each of which is allocated an identifier having a predetermined number of bits (Jaeckel: C 10, L 5-16; EN: Having not further defined the applicant's claimed "identifier" in the claimed invention, the examiner has found that the claimed "identifier" reads on the coordinates taught by Jaeckel.), each bit having first and second selectable states, a data memory having a plurality of word lines of predetermined length (Jaeckel: C 20, L 10-11), each of the said address decoders being activatable to select one of the plurality of word lines (Jaeckel: C 11, L 55-61; EN: The examiner takes the position that Jaeckel anticipates the applicant's claimed address decoders being "activatable to select" in teaching his address decoders being activated to select hard memory locations which contain word lines.), means to

receive an input address (Jaeckel: C 19, L 19-28; EN: Having not further defined the applicant's claimed "means to receive" in the claimed invention, the examiner has found that the claimed "means to receive" reads on the AND-Gate which makes up the address decoders as taught by Jaeckel.), and means to activate one or more of the address decoders if a comparison between a decoder identifier and the input address exceeds a predetermined comparison threshold (Jaeckel: C19, L 19-27 and C 20, L 7-17; EN: The examiner takes the position claimed "means to activate" is inherent in the invention of Jaeckel. This position is based on Jaeckel teaching the comparing of inputs into an address decoder with the coordinates of the address decoder, and activating the decoder if all ten coordinate values match, where the ten coordinate values matching is the "threshold".),

determining an operationally beneficial number of address decoders to be activated in response to a valid input address (Jaeckel: C 4, L 18-27; EN: The examiner takes the position that the plurality of address decoders being a "operationally beneficial number" is inherent in the invention of Jaeckel.), and

Ichiriu teaches

configuring the comparison threshold such that a valid input address will activate a number of address decoders substantially equal to the operationally beneficial number of address decoders to be activated (Ichiriu: C 5, L 17-20; EN: The examiner takes the position that Ichiriu anticipates the applicant's claimed "configuring", in teaching the use of valid and non-valid words, and the use of a highest priority match register, which only

activates the address decoders for the words which generate the highest matches when compared to input addresses.).

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the memory system of Jaeckel with the memory of Ichiriu for the purpose of activating an operationally beneficial number of address decoders based on a comparison threshold (Ichiriu: C 5, L 17-20).

Regarding claims 22:

Jaeckel teaches

(Original) A method wherein the comparison compares the number of bits set to the first selectable state in the input address with the number of bits set to the first selectable state in each of the address decoder identifiers (Jaeckel: C 11, L 4-7).

Regarding claims 23:

Jaeckel does not explicitly teach the operationally beneficial number being determined so as to allow maximum error free data recovery from the data memory

However, Ichiriu does teach,

(Previously Presented) A method wherein the operationally beneficial number is determined so as to allow maximum error free data recovery from the data memory (Ichiriu: EN: The examiner takes the position that the highest priority match method of determining which address decoders to activate, is for the purpose of minimizing error in data recovery and storage. This position is supported by Ichiriu et al. teaching that his

invention is for error detection in Column 1, Lines 13-15, teaching the exclusion of error addresses in Column 7, Lines 1-8, and the matching of highest priority words in Column 5, Lines 17-21).

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the memory system of Jaeckel with the memory of Ichiriu for the purpose of error free data recovery (Ichiriu: C 1, L 13-15).

Allowable Subject Matter

Claims 24-29 which are not been rejected under the prior art, would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and upon traversal of any rejections or objections found in any base claim or any intervening claims.

Conclusion

Claims 1-31 and 35-36 are rejected.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adrian L. Kennedy whose telephone number is (571) 270-1505. The examiner can normally be reached on Mon -Fri 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Vincent can be reached on

(571) 272-3080. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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ALK

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